VALIDATION OF ELECTRICAL PERFORMANCE OF AN ELECTRONIC PACKAGE PRIOR TO FABRICATION

Abstract of the Disclosure

An electrical resistance determination method. Input to the method includes a description of at least one electrical network within a substrate. The description includes specification of a plurality of first ports on a first side of the substrate, and a plurality of second ports on a second side of the substrate, for each electrical network. All of the first ports are electrically isolated from one another. All of the second ports are electrically connected to a common voltage. A computer readable program code, which is executed by a processor of a computer system computes for a first electrical network of the at least one electrical network an electrical resistance between each first port and a port of the second ports. The computer code may also display a perspective plot of the computed electrical resistances as a bar oriented about normal to each first port.